Address	0xF0			SERIAL TX BUFFER				
Bit	7	6	5	4	3	2	1	0
Name	txdata_7	txdata_6	txdata_5	txdata_4	txdata_3	txdata_2	txdata_1	txdata_0
Type	W	W	W	W	W	W	W	W

Bit(s)		Name	Description
7:0		txdata_x	Data bit
			0: Bit not set
			1: Bit set

Example				Uppercase "A"				
Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	1	0	1

Address	0xF1			SERIAL RX BUFFER				
Bit	7	6	5	4	3	2	1	0
Name	rxdata_7	rxdata_6	rxdata_5	rxdata_4	rxdata_3	rxdata_2	rxdata_1	rxdata_0
Type	R	R	R	R	R	R	R	R

Bit(s)		Name	Description
7:0		rxdata_x	Data bit
			0: Bit not set
			1: Bit set

Example				Uppercase "A"				
Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	1	0	1

Address	0xF2			SERIAL IRQ ENABLE				
Bit	7	6	5	4	3	2	1	0
Name	TxEmpty_EN	RxEmpty_EN	TxTrg_EN	RxTrg_EN	-	-	-	-
Type	RW	RW	RW	RW	R	R	R	R

Bit(s)		Name	Description
7:0		xxxx_EN	Enable bit
			0: IRQ not enabled
			1: IRQ enabled

Example				TX Data FIFO Empty IRQ and TX Data FIFO Trigger are enabled				
Bit	7	6	5	4	3	2	1	0
	1	0	1	0	ND	ND	ND	ND

Address	0xF3			SERIAL IRQ				
Bit	7	6	5	4	3	2	1	0
Name	TxEmpty	RxEmpty	TxTrg	RxTrg	-	-	-	-
Type	RW	RW	RW	RW	R	R	R	R

Bit(s)		Name	Description
7:0		xxxx	IRQ Status
			0: IRQ not present
			1: IRQ Present

Example				TX Data FIFO Epty IRQ				
Bit	7	6	5	4	3	2	1	0
	1	0	0	0	ND	ND	ND	ND

Address	0xF4			SERIAL MODE				
Bit	7	6	5	4	3	2	1	0
Name	Tx_DISABLE	Rx_DISABLE	-	RxEmtyInv	-	-	-	FIFO_flush
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit(s)		Name	Description
7:6		xxx_DISABLE	Communication status
			0: Communication enabled
			1: Communication Disabled

Bit(s)		Name	Description
4		RxEmtyInv	If set the IRQ is generated when data is added on empty buffer
			0: Communication enabled
			1: Communication Disabled

Bit(s)		Name	Description
0		FIFO_flush	If set the FIFOs are flushed (See Serial.flush()), than this bit is set back to 0
			0: Normal Operation
			1: Flush FIFOs

Example				TX and RX are enabled, generate IRQ whenEMPTY RX FIFOs is filled

Bit	7	6	5	4	3	2	1	0
	0	0	ND	1	ND	ND	ND	0

Address	0xF5			SERIAL TRIGGER LEVEL				
Bit	7	6	5	4	3	2	1	0
Name	TxLvl_3	TxLvl_2	TxLvl_1	TxLvl_0	RxLvl_3	RxLvl_2	RxLvl_1	RxLvl_0
Type	RW	RW	RW	RW	RW	RW	RW	RW

Bit(s)		Name	Description
7:4		TxLvl	Transmission divider, Ring buffer divided by this value + 1
3:0		RxLvl	Receiver divider, Ring buffer divided by this value + 1

Example				TX and RX trigger level is divided by 16. if the buffer is 64 bytes trigger is at 4 bytes.				
Bit	7	6	5	4	3	2	1	0
	1	1	1	1	1	1	1	1

Address	0xF6			SERIAL LINE SPEED				
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	Baud_3	Baud_2	Baud_1	Baud_0
Type	R	R	R	R	RW	RW	RW	RW

Bit(s)		Name	Description
2:0		Baud	Baud rate
			000: 4800
			001: 9600
			010: 11400
			011: 19200
			100: 28800
			101: 38400
			110: 57600
			111: 115200

Example				9600 baud				
Bit	7	6	5	4	3	2	1	0
	ND	ND	ND	ND	0	1	1	1

Address	0xF7			SERIAL LINE CONFIG				
Bit	7	6	5	4	3	2	1	0
Name	-	-	BitParity_1	BitParity_0	StopBit	WordLen_1	WordLen_0	-
Type	R	R	RW	RW	RW	RW	RW	R

Bit(s)		Name	Description
5:4		BitParity	Bit parity: ODD, EVEN or DISABLED
			00:Disabled
			01: Reserved
			10: Enabled, Even Parity
			11: Enabled, Odd Parity

Bit(s)		Name	Description
3		StopBit	If set the STOp bit is 2 otherwise it's 1
			0: 1 STOP bit
			1: 2 Stop bits

Bit(s)		Name	Description
2:1		WordLen	Word data length
			00: Word Lenght of 5 bits
			01: Word Lenght of 6 bits
			10: Word Lenght of 7 bits
			11: Word Lenght of 8 bits

Example				Data format: 8N1				
Bit	7	6	5	4	3	2	1	0
	ND	ND	0	0	0	1	1	ND